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A New Design of Low Power Hybrid CMOS Full Adder

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Abstract— *The new Full Adder is designed by dividing the full adder design in three modules, which is called hybrid-CMOS logic style. By using this design style we can optimize our design at various levels and full adder can be designed according to the circuit requirement. In first module a XOR-XNOR circuit, which generates full swing XOR and XNOR outputs simultaneously, is used. XOR-XNOR circuit used in first module must have good driving capability. We can use the first module circuit with minimum power requirement and minimum delay for getting the best result after next stage. In second module a sum circuit is used which is also a XOR circuit and uses the output of first module and carry as input and generate sum output. Third module is a carry circuit, which also uses the output of first stage according to requirement to generate carry output.*

The new full adder design is based on XOR-XNOR circuit according to the requirements. A new proposed sum circuit and a new proposed carry circuit reduce the power consumption and delay with respect to carry and PDP 12-125%. Simulations are carried out on HSPICE using TSMC 0.18 µm CMOS technology. To evaluate the performance of the new full adder circuit in a real circuit environment, we embedded it in a 4- and 8-bit, parallel adder chain. The new adder displayed better performance as compared to the standard full adders of this logic style.

Index Terms- *Adder; Hybrid-CMOS logic style; Low Power; High Speed*

1. INTRODUCTION

Full adder is a basic building block for various arithmetic circuits such as multipliers, compressors, comparators and so on. The power requirement and output delay of these circuits is greatly depend upon the power requirement and delay of full adder circuits. So by minimizing the power and delay of the full adder circuit we can design high performance arithmetic circuits.

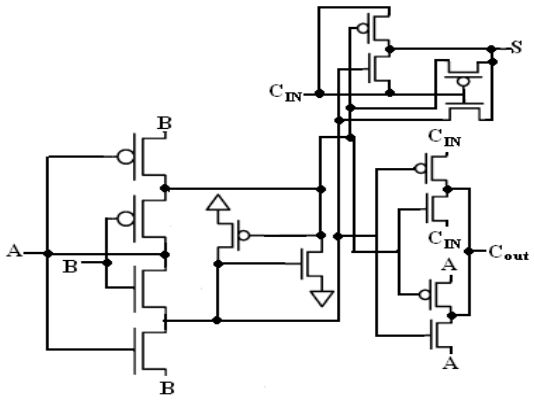
Several logic styles for designing the Full adder have been proposed. Each style has some advantages and some disadvantages. In classical design of full adder normally single CMOS structure is used for whole design. Such as the standard static CMOS full adder[4] is based on regular CMOS structure with conventional pull-up and pull-down transistors providing full swing output and good driving capabilities. The main drawback of this circuit is high input capacitance and use of large no. of PMOS, due to which the speed of this structure is degrade. In another conventional design the complementary pass transistor logic (CPL)[4] is used. It provides good driving capability, full swing of operation and high speed. But its main disadvantage is high power dissipation due to large number of internal nodes in the cell. The speed of dynamic CMOS logic style adder is higher. It has several demerits such as charge sharing, high clock load, higher switching activities and lower noise immunity. And it requires high power requirement for driving the clock lines. Another logic styles are transmission-gate full adder (TGA)[5] and transmission-function full adder (TFA)[6] based upon transmission gates and transmission function theory. These full adders are very low power consuming but have very low driving capabilities.

Hybrid-CMOS logic design style uses more than one module for designing of full adder. Examples of this style are NEW 14-T adder [7], hybrid pass logic with static CMOS output drive (HPSC) full adder [8], NEW-HPSC [9] full adder and hybrid-CMOS full adder[10]. In this design style full adder structure is designed by breaking the full adder into three modules. In module I a XOR-XNOR circuit is designed. The outputs of module I is used as intermediate signals for the other modules. So it is required to get full output swing of XOR and XNOR simultaneously and circuit must have good driving capability. Module II and Module III are the sum and carry circuits which use the intermediate signals and third input signal as input to produce the sum and carry respectively. The structures of standard hybrid-CMOS full adder cells are shown in fig.1.

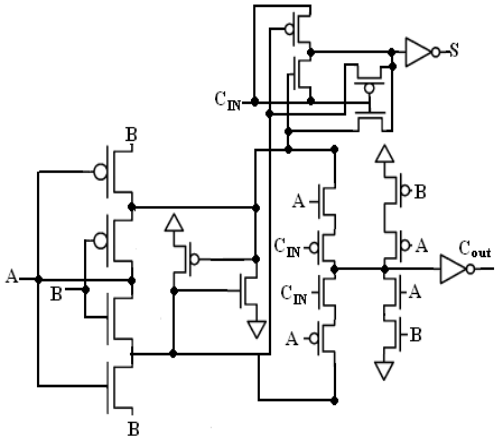
This logic design style provides the freedom to take the optimum circuits for every module for getting the optimum performance of adder cell. These adders generally lack the driving capabilities. Their performance as a single bit is good but as the size of chain increases, the performance degraded drastically. But we tried to present an adder with this logic style for which the performance is not degraded in adder chain.

In this paper we use the XOR-XNOR circuit which is best according to our requirements of full XOR and XNOR output swing and good driving capability and present a new sum circuit, used as module II and a new carry circuit, used as module III. These circuits use the XOR and XNOR of two signals and third signal (carry input) as input in full adder design and give the sum output and carry output (Cout). We tried to get better delay performance between Cout and Cin.

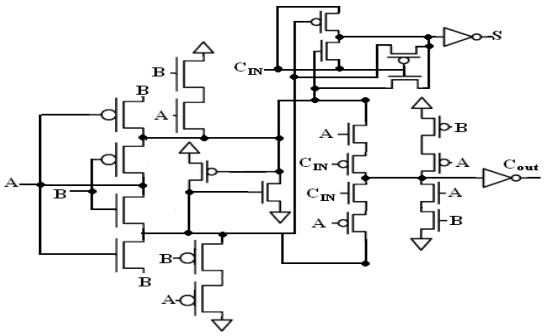
In the recent year many other new circuits are proposed using less number of transistors with less delay and very low power requirement. An adder with 10 transistors[12],[15] an adder with 8 transistors[16] do not give full swing outputs for all input combinations and there is difference in output level for different combinations and these circuits have very low driving capabilities. Some other circuits are also proposed in [13] but they do not give full swing output and power requirement is more. We do not take these adders in our discussion due to the do not provide full swing output.



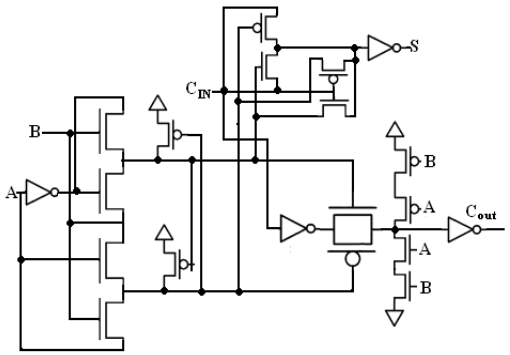
(a)NEW-14 T adder



(b) HPSC adder



(c) NEW-HPSC adder



(d) Hybrid-CMOS adder

Fig. 1: Standard existing full adder cells

2. PROPOSED CIRCUIT

In the prop**o**sed circuit we use three modules some circuits of require full XOR and XNOR output swing simultaneously and good driving capability.there are many proposed XOR-XNOR circuits but many of them do not meet our requirements.

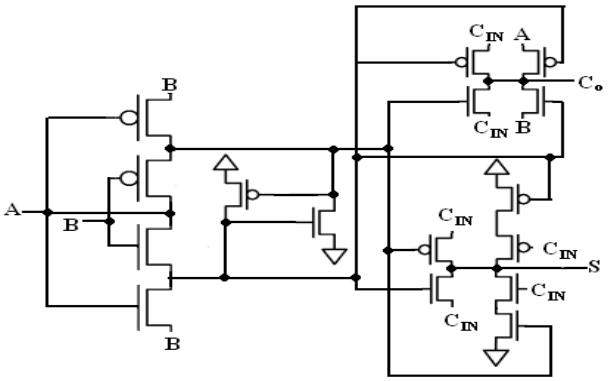


Fig. 2: Proposed full adder

We use hybrid CMOS logic style to design a new proposed full adder circuit as shown in Fig.2. This circuit has three modules. In module I we use a XOR-XNOR circuit. It produces XOR and XNOR outputs with full swing simultaneously as intermediate signals for other modules. Module II circuit, produces sum output using intermediate signals produce by module I and third input (C_{IN}). Module III circuit, produces carry output using intermediate signals of module I and input signals A, B, and C_{IN}.

3. SIMULATION RESULTS

3.1 Simulation Setup:

The transient analyses of the circuits were performed on HSPICE at a supply voltage ranging 1.2V-2.4V using TSMC

0.186m CMOS process technology. For providing the real environment to the simulation. we use input buffers for all the inputs and a constant output load capacitance of 5.6fF for power and delay measurements. Comparison of the worst case C_{IN} to C_{OUT} delay, C_{IN} to C sum output delay, power consumption, PDP for sum and carry outputs at the supply voltage range of 1.2V-2.4V of reported and proposed circuit is shown in Fig.4, 5, 6 and 7.

3.2 Simulation Results and Discussion:

The delay comparison of carry in (C_{IN}) to carry out (V. Simulation results The proposed circuit provides the better delay performance than the reported circuits in Fig. 1 in terms of worst case C_{IN} to C_{OUT} delay. The proposed circuit is 55% to 57% faster than other reported circuits in Fig.1 at 1.8V supply voltage

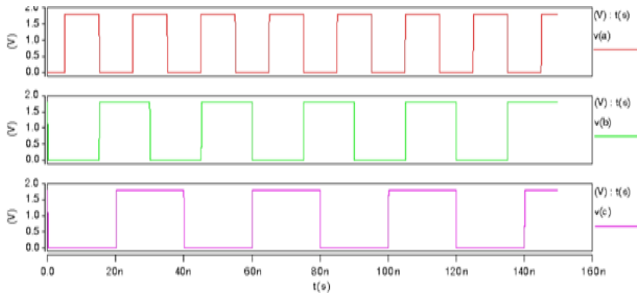


Fig. 3a: Input waveforms for the proposed circuits

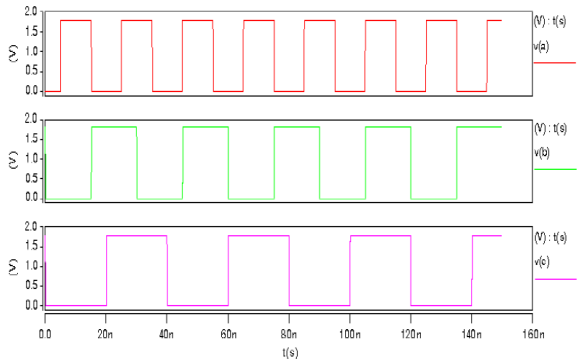


Fig.3b: output waveforms for the proposed circuits

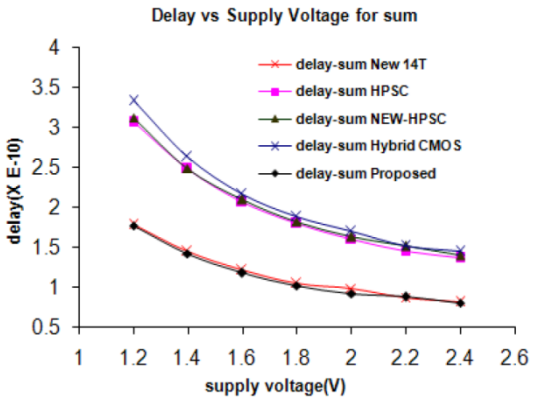


Fig.4: Delay sum comparision for different circuits

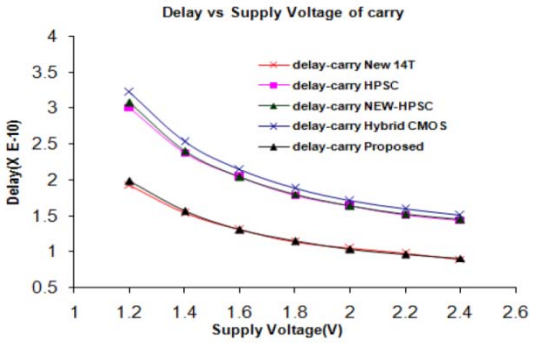


Fig. 5: Delay carry comparision for different circuits

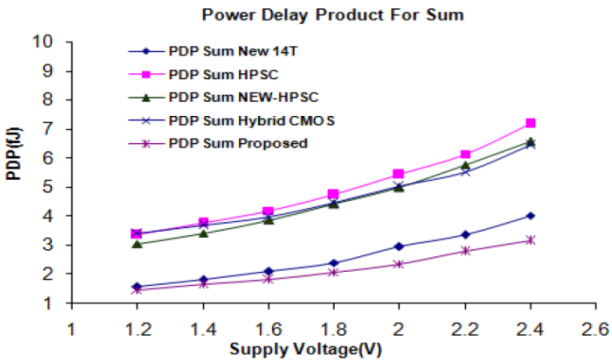


Fig. 6: PDP sum comparision for different circ

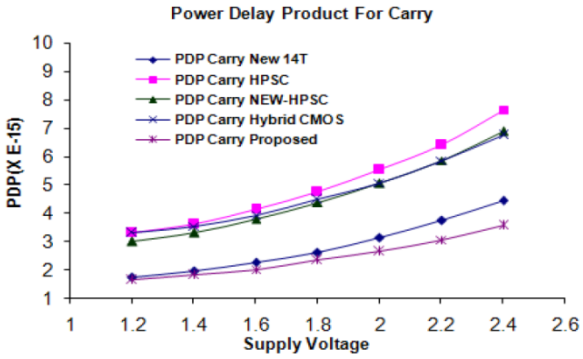


Fig.7: PDP carry comparision for different circuits

4. CONCLUSION

Hybrid-CMOS design style gives more freedom to the designer to select different modules in a circuit depending upon the application. Using the adder categorization and hybrid-CMOS design style, many full adders can be conceived. As an example, a novel full adder designed using hybrid-CMOS design style is presented in this paper that targets low PDP. The proposed hybrid-CMOS full adder has better performance than most of the standard full-adder cells owing to the novels design modules proposed in this paper. It performs well with supply voltage ranging from 1.2V to 2.4V. When embedded in a parallel adder chain, it outperforms all the other adders making it suitable for larger arithmetic circuits.

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